LCDD GEN3

DATASHEET

THE LCD DRIVER TESTER

KEY FEATURES

- Cost-optimized
- Large panel LCD driver test
- High speed interface for mLVDS/P2P/MIPI
- CP/FT(COF included) test solution
- Easy maintenance
- Ultimately compatible design

THE MOST COST/PERFORMANCE-OPTIMIZED
LCD DRIVER TESTER IN THE INDUSTRY

ABOUT THE LCDD GEN3

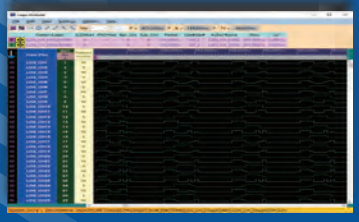
Inheriting the outstanding design of V50 and S100, YTEC launched a new test system LCDD Gen.3 for LCD driver testing. With intuitive and powerful engineering tools LCDD Gen.3 shortens test program development time for clients, which means improving client's time to market. And to lower client's cost LCDD Gen.3 is designed to be compatible with other platform, not only accessory but also mechanism. It is definitely one of the most cost-optimized LCD driver test system in the industry.

- 2,400 LCD grayscale channels
- 2.5G HSIF lanes
- User-friendly interface with powerful engineering tools
- Ultimately compatible design (accessory and mechanism)

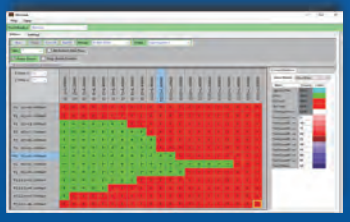
YTEC

YOUNGTEK ELECTRONICS CORP.

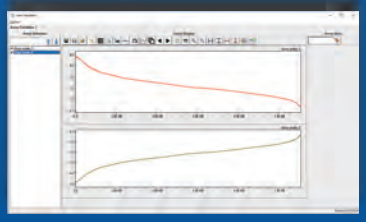
POWERFUL SUITE OF SOFTWARE TOOLS



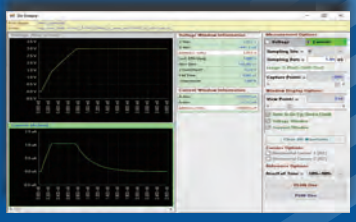
LA TOOL



SHMOO TOOL



ARRAY VIEWER



SCOPE TOOL

SPECIFICATIONS

MAX PIN COUNT	Normal IO: 256 / LCD: 2,400 / HS LANE:24
MAX MULTI SITE TEST	8
MAX TEST RATE	Normal IO: 100MHz / HS: 2.5Gbps
PATTERN MEMORY	128M
Digital BD	128 PE CH / 16 PMU / 8 TMU
HS BD	8 HS LANE / 8 VS / 32 RVS
LCD BD	600 LCD CH
CMP BD	192 CMP CH
DEVELOP ENVIRONMENT	WIN10, C/C++
USER POWER ON/OFF	SOFTWARE CONTROLLED
SYNC MECHANISM	LOG BOARD @ SLOT1 AS MASTER
DIRECT MOUNT SOLUTION	YES
USER RELAY	128
USER POWER	-5.2V, +5V, ±15V
POWER CONSUMPTION	3,500 W
DIMENSIONS	L: 90.00cm, W: 83.00cm, H: 81.95cm
WEIGHT	250KG (all boards equipped)
COF SOLUTION	YES
APPLICATION	LCD Driver / TDDI / Automotive

Versatile function to accommodate all kinds of LCD driver IC application.	
MAX PIN COUNT	Normal IO: 256 / LCD: 2,400 / HS LANE:24
MAX MULTI SITE TEST	8
MAX TEST RATE	Normal IO: 100MHz / HS: 2.5Gbps
PATTERN MEMORY	128M
VS	24
RVS	48

Digital BD	
PE CH	128
TEST RATE	100MHz
VIL/VIH	-2V ~ +7V
VOL/VOH	-2V ~ +7V
ACTIVE LOAD	±24mA
NUMBER OF EDGES	4
EPA	±500ps
PATTERN MEMORY	128M
SCAN CHAIN	1 CHAIN < 4096M 4 CHAIN < 1024M
TMU RANGE	MAX 300MHz
PMU	±10V, ±500mA
PPMU	-2V ~ +7V, ±32mA

HS BD	
HS LANE	8(1.6Gbps) / 6 (2.5Gbps)
TEST RATE	2.5Gbps
VIL/VIH	-0.5V ~ +3V
PATTERN MEMORY	128M
VS	±24V, ±400mA
RVS	±24V, ±100mA

LCD BD	
LCD CH	600
INPUT RANGE	E1: ±10V E2: 0V ~ 20V E3: -2V ~ 18V
ACCURACY	±3.5mV
ACQ MEMORY	8K
INPUT IMPEDANCE	500MΩ
DIGITIZER	16 bits
MINIMUM CONVERSION	6us
ACTIVE LOAD	±1mA

CMP BD	
CMP CH	192
INPUT RANGE	-16V ~ 21V

ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

YTEC
PHONE: + 886 3-666-9968 WEB: WWW.YTEC.COM.TW

YOUNGTEK ELECTRONICS CORP.
4F, NO. 5, KEJI RD.
SCIENCE-BASED INDUSTRIAL PARK
HSINCHU CITY 30078 TAIWAN